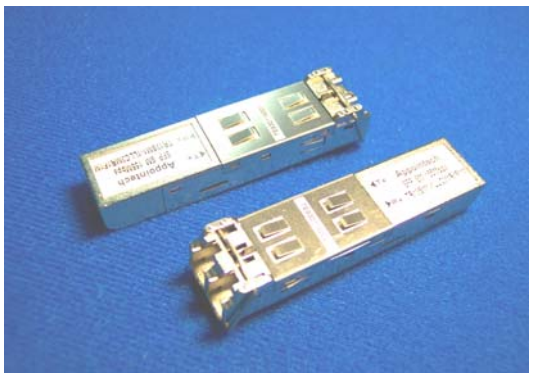
Singlemode 1.25Gbps CWDM Optical Transceiver
SFP with Digital Diagnostic

Features



- Compliant with SFP MSA and SFF-8472(Rev 9.3)
- Compliant with IEEE 802.3z Gigabit Ethernet 1000BASE-LX specification
- SFF-8472 Digital Diagnostic Monitoring Interface with real time monitors
  - Transmitter Output Power
  - Receiver Input Power
  - Laser Bias Current
  - Temperature
  - Supply Voltage
- Internal calibration for Digital Diagnostic Monitoring
- Alarms and warnings to indicate status of real time monitors
- Metal case & LC duplex receptacle with bail de-latch
- Transmitter disable input and receiver loss of signal output
- Wide operating temperature range –40℃~85℃
- Single 3.3V power supply
- AC coupled LVPECL compatible data input and output
- 2-wire serial EEPROM protocol

Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Transmitter					
Data Rate (NRZ)	B	-	1250	-	Mb/s
Optical Output Power (avg.) (1) (2) (3)					
-1	P_o	-11	-	-6	dBm
-2	P_o	-5	-	0	dBm
-3	P_o	-3	-	+2	dBm
Extinction Ratio (2)	ER	9	-	-	dB
Optical Wavelength					
CWDM DFB	λ_C	1270	-	1610	nm
Spectral Width	$\Delta\lambda$	-	-	1	nm
Side Mode Suppression Ratio	SMSR	30	-	-	dB
Output Rise Time (20-80%) (2)	t_r	-	-	260	ps
Output Fall Time (20-80%) (2)	t_f	-	-	260	ps
Data Differential Input Voltage	V_i	500	-	2400	mV_{p-p}
TX Fault Output Voltage	V_{FOL} V_{FOH}	0 2.4	- -	0.4 Vcc	V

Parameter	Symbol	Min.	Typ.	Max.	Unit
TX Disable Input Voltage	V_{DIL} V_{DIH}	0 2	- -	0.8 Vcc	V
Supply Voltage	Vcc	2.97	3.3	3.63	V
Supply Current	Icc	-	-	150	mA

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Receiver					
Data Rate (NRZ)	B	-	1250	-	Mb/s
Optical Input Sensitivity (avg.) (1) (2) (5)					
-1	P_{IN}	-	-	-20	dBm
-2	P_{IN}	-	-	-23	dBm
-3	P_{IN}	-	-	-32	dBm
Saturation (avg. power)	P_{SAT}	-3	-	-	dBm
Optical Wavelength	λ	1100	-	1600	nm
Output Rise Time (20-80%)	t_r	-	-	250	ps
Output Fall Time (20-80%)	t_f	-	-	250	ps
Data Differential Output Voltage	V_o	370	-	2000	mV_{p-p}
LOS Deasserted Power Level (avg.)	P_A	-	-	-20	dBm
LOS Asserted Power Level (avg.)	P_D	-35	-	-	dBm
LOS Hysteresis	P_{HYS}	0.5	3	-	dB
LOS Output Voltage	V_{LOS-OL} V_{LOS-OH}	0 2.4	- -	0.4 Vcc	V
Supply Voltage	Vcc	2.97	3.3	3.63	V
Supply Current	Icc	-	-	130	mA

Notes：

(1) With 0.275 NA, 9/125μm fiber.
(2) Compliant to IEEE802.3z Gigabit Ethernet 1000BASE-LX.
(3) Class 1 eye safe per FDA and IEC.
(4) Transmitter eye mask diagram is compliant to IEEE802.3z Eye Diagram.
(5) 2^7 -1 PRBS, BER= 10^{-12}.
(6) The transmitter output should not be viewed directly.

Absolute Maximum Ratings

Parameter		**Min.**	**Max.**	**Unit**
Operating Temperature	-1	0	70	°C
	-2	-40	85	°C
Storage Temperature		-40	100	°C
Lead Soldering Limits		-	240/10	°C /sec
Supply Voltage		-0.5	4	V

Digital Diagnostic Monitor Characteristics

Parameter	**Min.**	**Unit**
Transceiver Internal Temperature Accuracy	±3.0	°C
Transceiver Internal Supply Voltage Accuracy	±3	%
TX Laser Bias Current Accuracy	±1 0	%
TX Average Output Power Accuracy	±3.0	dB
RX Average Input Power Accuracy	±3.0	dB

Timing of Control and Status I/O

Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Condition**
TX Disable Assert Time	t_off		10	μs	Time from rising edge of TX Disable to when the optical output falls below 10% of nominal.

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TX Disable Negate Time	t_on		1	ms	Time from falling edge of TX Disable to when the modulated optical output rises above 90% of nominal.
Time to initialize, including reset of TX_Fault	t_init		300	ms	From power on or negation of TX Fault using TX Disable.
TX Fault Assert Time	t_fault		100	μs	Time from fault to TX fault on.
TX Disable to reset	t_reset	10		μs	Time TX Disable must be held high to reset TX_fault.
LOS Assert Time	t_loss_on		100	μs	Time from LOS state to RX LOS assert.
LOS Deassert Time	t_loss_off		100	μs	Time from non-LOS state to RX LOS deassert.
Serial ID Clock Rate	f_serial_clock		100	kHz	

Ordering Information

T R □ □ S M 3 - □ F L C 3 M R □ F □ D

Operating Temperature Range：
1：0°C ~ 70°C
2：-40°C ~ 85°C

Sensitivity Grade：
(refer to Specifications)
1：-1
2：-2　3: -3

Laser Type：
F：DFB LD

Tx Output Power Grade：
(refer to Specifications)
1：-1
2：-2
3：-3

Wavelength：
1270 ~ 1610nm CWDM Grid

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Part Number	Laser Type	Power Budget (1)	Recommended Maximum Reach (2)	Compliant to Gigabit Ethernet (4)
TR13SM3-1LLC3MR1F□D	1310nm, FP	9dB	17Km	1000BASE-LX
TR13SM3-2LLC3MR2F□D	1310nm, FP	18dB	42Km	-
TR15SM3-3FLC3MR2F□D	1550nm, DFB	20dB	68Km	-

Notes：

(1) Power Budget (min.) = TX Output Power (min.) - RX Sensitivity (min.)
(2) Assuming connector loss 3dB; 1310nm fiber attenuation coefficient 0.35dB/Km; 1550nm fiber attenuation coefficient 0.25dB/Km.
(3) The maximum reach value is recommended, not guaranteed. The exact transmission distance depends on fiber loss, connector loss and system penalty.
(4) Gigabit Ethernet standard specification is defined in IEEE802.3z.

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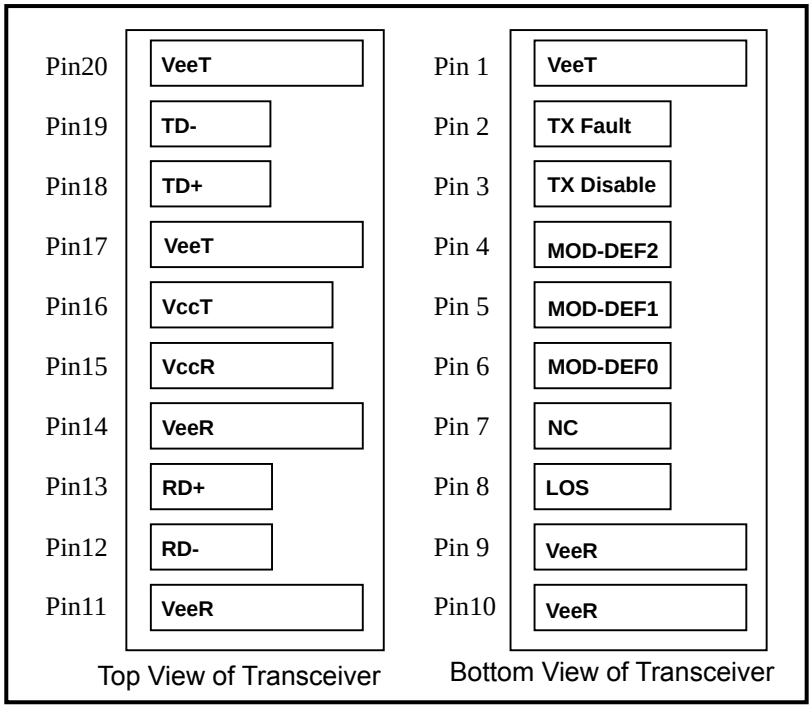
Outline Drawing

UNIT：mm

SFP Transceiver Electrical Pad Layout



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Pin Description

Pin No.	Symbol	Description
1	VeeT	Transmitter Ground
2	TX Fault	Transmitter Fault Indication Logic Low indicates normal operation. Logic High Indicates a laser fault of some kind. TX Fault is an open drain output, which should be pulled up with a 4.7K – 10KΩ resistor on the host board.
3	TX Disable	Transmitter Disable Its states are： Low (0 – 0.8V) ：Transmitter on (>0.8, < 2.0V) ：Undefined High (2.0 – 3.465V) ：Transmitter Disabled Open ：Transmitter Disabled It is pulled up within the module with a 4.7K – 10 K.Ω resistor.
4	MOD-DEF2	Module Definition 2 (SDA) The data line of two wire serial interface for serial ID. MOD-DEF2 should be pulled up with a 4.7K – 10KΩresistor on the host board. The pull-up voltage shall be VccT or VccR.
5	MOD-DEF1	Module Definition 1 (SCL) The clock line of two wire serial interface for serial ID. MOD-DEF1 should be pulled up with a 4.7K – 10KΩresistor on the host board. The pull-up voltage shall be VccT or VccR.
6	MOD-DEF0	Module Definition 0 (WP) MOD-DEF0 is grounded by the module to indicate that the module is present.
7	NC	Not connected
8	LOS	Loss of Signal Logic High indicates the received optical power is below the worst-case receiver sensitivity. Logic Low indicates normal operation. LOS is an open drain output, which should be pulled up with a 4.7K – 10KΩ resistor on the host board.
9	VeeR	Receiver Ground
10	VeeR	Receiver Ground
11	VeeR	Receiver Ground
12	RD-	Inv. Received Data Out (Note 1)
13	RD+	Received Data Out (Note 1)
14	VeeR	Receiver Ground
15	VccR	Receiver Power Supply
16	VccT	Transmitter Power Supply
17	VeeT	Transmitter Ground
18	TD+	Transmitter Data In (Note 2)
19	TD-	Inv. Transmit Data In (Note 2)
20	VeeT	Transmitter Ground

Notes：

1. RD+ and RD- are AC coupled 100Ω differential lines which should be terminated with 100Ω (differential) at the user SERDES. The AC coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 370 and 2000 mV differential (185 – 1000 mV single ended) when properly terminated.
2. TD+ and TD- are AC-coupled, differential lines with 100Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 – 2400 mV (250 – 1200 mV single-ended), though it is recommended that values between 500 and 1200 mV differential (250 – 600 mV single-ended) be used for best EMI performance.

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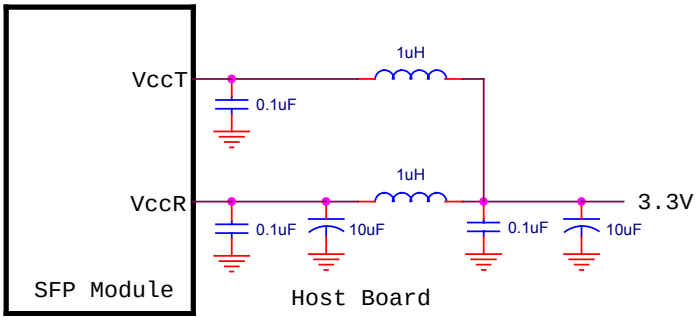
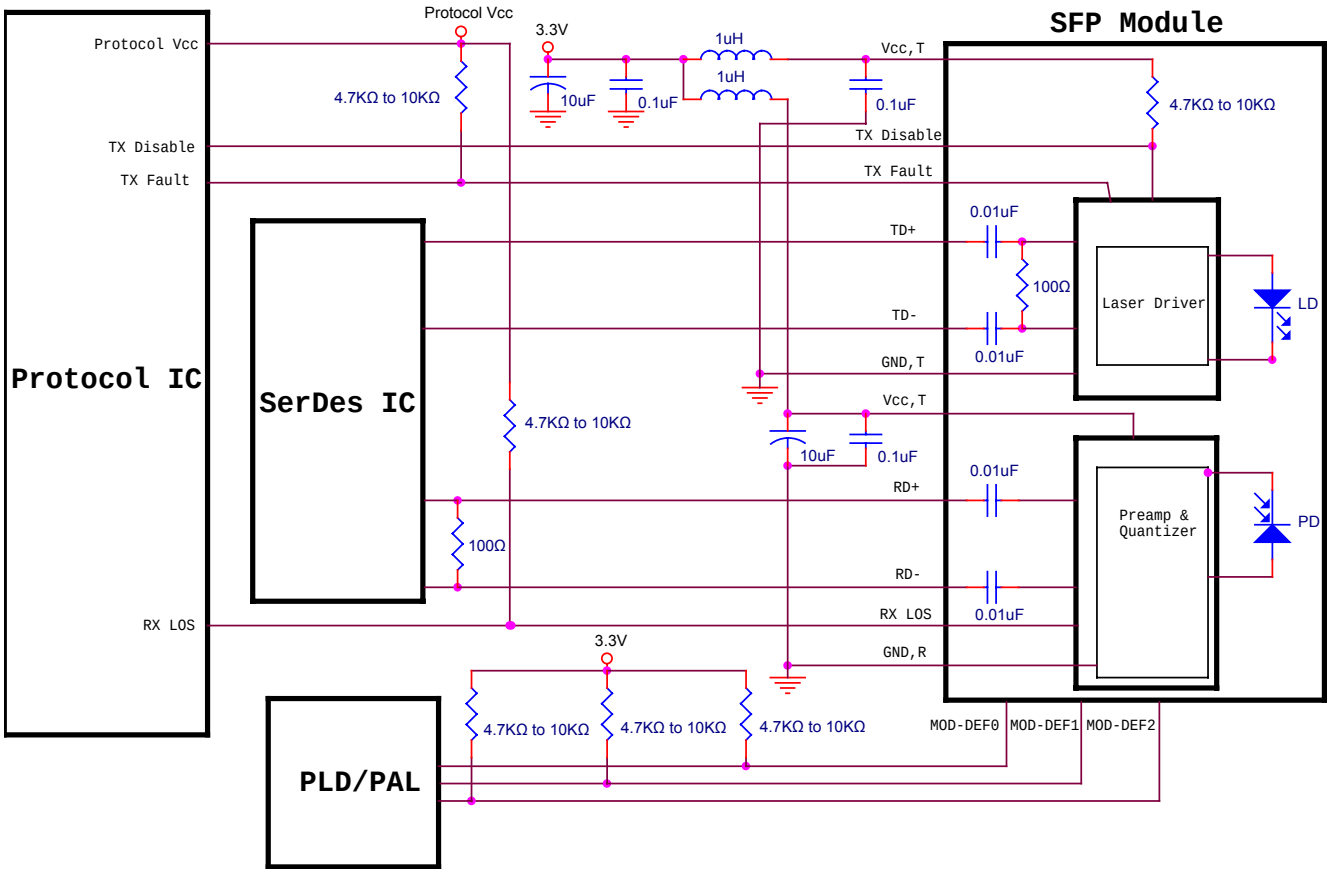
Recommended Host Board Supply Filtering Network



Example SFP Host Board Schematic



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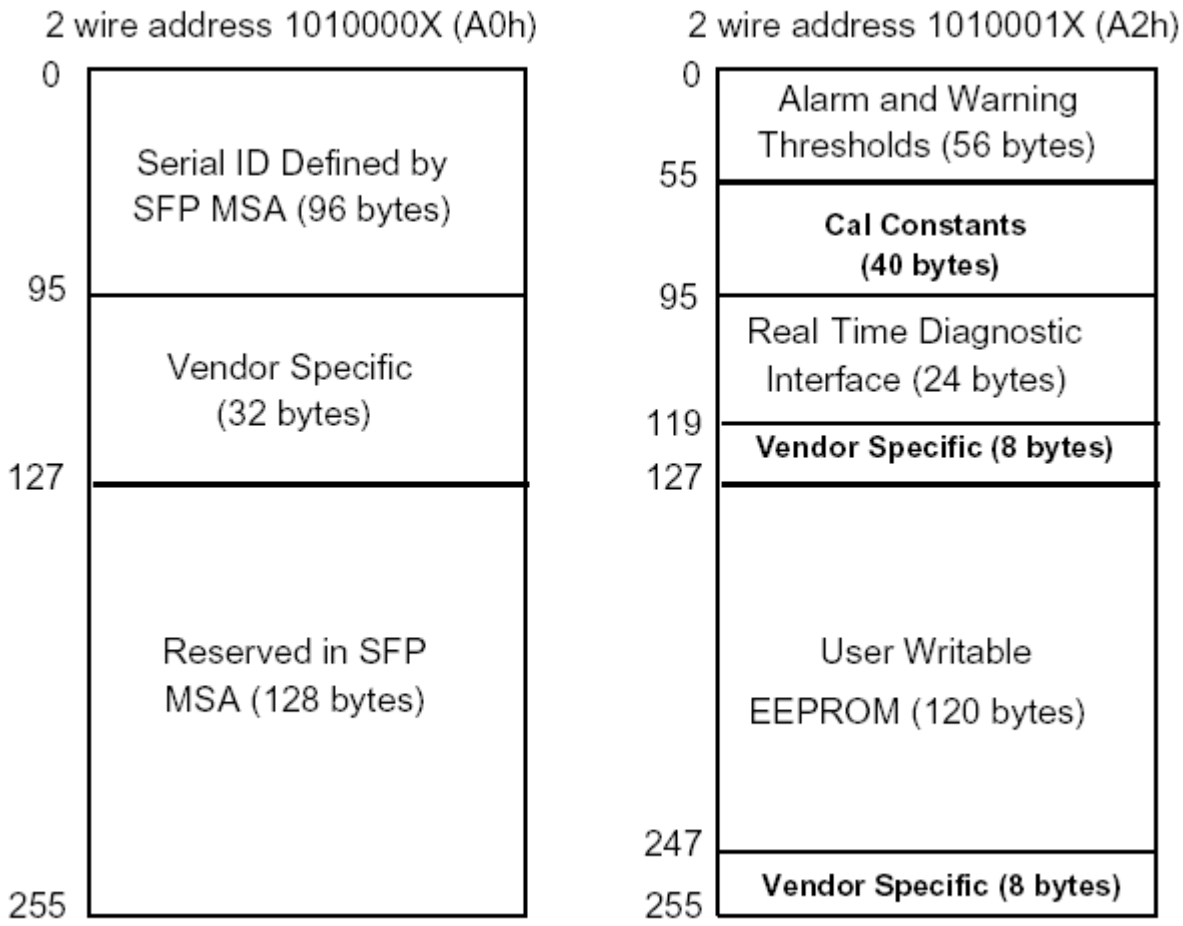
Memory Map



EEPROM Serial ID Memory Contents (A0h)

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
0	03		32	20		64	00		96	20	
1	04		33	20		65	1A		97	20	
2	07		34	20		66	00		98	20	
3	00		35	20		67	00		99	20	
4	Note1		36	00		68	Note3		100	20	
5	Note1		37	20		69			101	20	
6	00		38	20		70			102	20	
7	00		39	20		71			103	20	
8	00		40	54	T	72			104	20	
9	00		41	52	R	73			105	20	
10	00		42	Note1	*	74			106	20	
11	05		43	Note1	*	75			107	20	
12	02		44	53	S	76			108	20	
13	00		45	4D	M	77			109	20	
14	Note1		46	33	3	78			110	20	
15	Note1		47	2D	-	79			111	20	
16	Note1		48	Note1	*	80			112	20	
17	Note1		49	Note1	*	81			113	20	
18	00		50	4C	L	82			114	20	
19	00		51	43	C	83			115	20	
20	41	A	52	33	3	84	Note4		116	20	
21	50	P	53	4D	M	85			117	20	
22	50	P	54	52	R	86			118	20	
23	4F	O	55	Note1	*	87			119	20	
24	49	I	56	46	F	88			120	20	
25	4E	N	57	20		89			121	20	
26	54	T	58	20		90			122	20	
27	45	E	59	20		91			123	20	
28	43	C	60	Note1		92	68		124	20	
29	48	H	61	Note1		93	B0		125	20	
30	20		62	00		94	01		126	20	
31	20		63	Note2		95	Note2		127	20	

Notes：

1. Data will vary depends on product.
2. Addresses 63 is check sum of bytes 0 – 62.
   Addresses 95 is check sum of bytes 64 – 94.
3. These addresses are reserved for serial number information.
4. These addresses are reserved for date code information.
5. The data transfer protocol and complete description of A0h memory contents are defined in SFP MSA and SFF-8472.

Digital Diagnostic

Alarm and Warning Thresholds (2-Wire Address A2h)

Address	#Bytes	Name	Description	Value
00-01	2	Temp High Alarm	MBS at low address	100°C
02-03	2	Temp Low Alarm	MBS at low address	-40°C
04-05	2	Temp High Warning	MBS at low address	+85°C
06-07	2	Temp Low Warning	MBS at low address	-35°C
08-09	2	Voltage High Alarm	MBS at low address	3.9V
10-11	2	Voltage Low Alarm	MBS at low address	2.7V
12-13	2	Voltage High Warning	MBS at low address	3.63V
14-15	2	Voltage Low Warning	MBS at low address	2.97V
16-17	2	Bias High Alarm	MBS at low address	70mA
18-19	2	Bias Low Alarm	MBS at low address	4mA
20-21	2	Bias High Warning	MBS at low address	60mA
22-23	2	Bias Low Warning	MBS at low address	5mA
24-25	2	TX Power High Alarm	MBS at low address	Note
26-27	2	TX Power Low Alarm	MBS at low address	Note
28-29	2	TX Power High Warning	MBS at low address	Note
30-31	2	TX Power LOW Warning	MBS at low address	Note
32-33	2	RX Power High Alarm	MBS at low address	Note
34-35	2	RX Power Low Alarm	MBS at low address	Note
36-37	2	RX Power High Warning	MBS at low address	Note
38-39	2	RX Power Low Warning	MBS at low address	Note
40-55	16	Reserved	Reserved for future monitored quantities.	

Note：Data value will vary depends on product.

Calibration constants for External Calibration Option (2-Wire Address A2h)

Address	#Bytes	Name	Description	Value (Note)
56-59	4	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power.	0
60-63	4	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power.	0
64-67	4	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power.	0
68-71	4	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power.	1
72-75	4	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power.	0
76-77	2	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current.	1
78-79	2	Tx_I(Offset)	Fixed decimal (signed two's complement) calibration data, laser bias current.	0
80-81	2	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power.	1
82-83	2	Tx_PWR(Offset)	Fixed decimal (signed two's complement) calibration data, transmitter coupled output power.	0
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature.	1
86-87	2	T (Offset)	Fixed decimal (signed two's complement) calibration data, internal module temperature.	0
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage.	1
90-91	2	V (Offset)	Fixed decimal (signed two's complement) calibration data, internal module supply voltage.	0
92-94	3	Reserved	Reserved	
95	1	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.	

Notes：The device is internally calibrated.

A/D Values and Status Bits (2-Wire Address A2h)

Byte	Bit	Name	Description
Converted analog values. Calibrated 16 bit data.			
96	All	Temperature MSB	Internally measured module temperature.
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver.
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias Current
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power.
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power.
105	All	RX Power LSB	
106	All	Reserved MSB	Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB	Reserved for 1st future definition of digitized analog input
108	All	Reserved MSB	Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB	Reserved for 2nd future definition of digitized analog input
Optional Status/Control Bits			
110	7	Tx Disable State	Digital state of the TX Disable Input Pin.
110	6	Soft Tx Disable	Read/write bit that allows software disable of laser. It is not implemented, the transceiver ignores the value of this bit.
110	5	Reserved	Reserved
110	4	RX Rate Select State	Digital state of the SFP RX Rate Select Input Pin.
110	3	Soft RX Rate Select	Read/write bit that allows software RX rate select. It is not implemented.
110	2	TX Fault	Digital state of the TX Fault Output Pin.
110	1	LOS	Digital state of the LOS Output Pin.
110	0	Data_Ready_Bar	Indicates transceiver has achieved power up and data is ready.
111	7-0	Reserved	Reserved

Alarm and Warning Flag Bits (2-Wire Address A2h)

Byte	Bit	Name	Description
Reserved Optional Alarm and Warning Flag Bits			
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
112	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
112	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
112	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
112	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
112	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
112	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
113	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
113	5	Reserved Alarm	
113	4	Reserved Alarm	
113	3	Reserved Alarm	
113	2	Reserved Alarm	
113	1	Reserved Alarm	
113	0	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
116	6	Temp Low Warning	Set when internal temperature is below low warning level.
116	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
116	4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
116	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
116	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
116	1	TX Power High Warning	Set when TX output power exceeds high warning level.
116	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.
117	6	RX Power Low Warning	Set when Received Power is below low warning level.
117	5	Reserved Warning	
117	4	Reserved Warning	
117	3	Reserved Warning	
117	2	Reserved Warning	
117	1	Reserved Warning	
117	0	Reserved Warning	
118	All	Reserved	

Vendor Specific Memory Addresses (2-Wire Address A2h)

Byte	Bit	Name	Description
120-127	All	Vendor Specific	Vendor Specific

User EEPROM (2-Wire Address A2h)

Address	#Bytes	Name	Description
128-247	120	User EEPROM	User writable EEPROM
248-255	8	Vendor Specific	Vendor specific control functions